## REMARKS

In the Office Action, the Examiner noted that the claims 1-30 are pending in the application and that the claims 1-30 are rejected over a prior art reference. By this response, no claims have been amended. Thus, claims 1-30 remain pending in the application. Applicant respectfully traverses the rejections for the reasons indicated below.

A. Interview Summary

The undersigned attorney and Rajesh Nair thank Examiner MacArthur for the courtesy of a telephone interview on December 12, 2006. The patentability of the pending claims over cited references (US 7,024,268 ("Bennett") and US 6,517,412 ("Lee")) were discussed. The feedback controlled polishing processes of Bennett was discussed. Applicant indicated that Bennett, Lee and Cambell do not suggest a model for CMP polishing of two or more layers, as required by the claimed invention. The details of the distinction between the cited art and the claimed invention are provided in the remarks that follow.

B. First Rejection under 35 U.S.C. §103(a)

Claims 1, 2, 4, 6, 10, 12, 13, 15, 17, 19, 23-26, 29, and 30 are rejected under 35 USC §103(a) as being obvious over Bennett et al. (US 7,024,268), hereafter "Bennett," in view of Lee et al (US 6,517,412), hereafter "Lee." Applicants respectfully traverse the rejection and respectfully submit that there is no motivation to combine the cited references to arrive at the presently claimed invention. Applicants discuss the rejection below as it applies to independent claims 1, 10, 23 and 30, and dependent claims 2, 4, 6, 12, 13, 15, 17, 19, 24-26 and 29.

The current invention is directed to methods and apparatus for polishing at least two layers of a wafer in a CMP process. Claim 1 recites "a model for CMP processing of a wafer having at least first and second layers comprising at least one control parameter, said *model comprising a first component that predicts a value for a characteristic of the first layer and a second component that predicts a value for a characteristic of the second layer*"; and "polishing at least first and second layers of a wafer" using a process recipe based on the model.

While Bennett and Lee disclose methods for polishing a wafer, nothing in the art of record discloses or suggests the controlled polishing of "at least two layers" of a wafer, much less a wafer CMP processing model that provides "a first component that predicts a value for a characteristic of the first layer and a second component that predicts a value for a characteristic of the second layer," as recited in claim 1.

Bennett provides feedback-controlled polishing of a *single metal layer.* Bennett discloses that "[d]uring each polishing cycle [of a metal layer], a first and second polishing process are sequentially performed on a current substrate." (Col. 5, lines 8-10). Bennett elsewhere teaches that the "first polishing process clears the first metal layer from the substrate during the first polishing cycle" and that the method calculates "clearing times of the first polishing process." (Col. 3, lines 3-7). According to Bennett, "[p]olishing proceeds at the second polishing station [] until the metal layer is removed and the underlying barrier layer is exposed" (Col. 10, lines 21-30). Although polishing of the metal layer can take place at two polishing stations, polishing at both polishing stations is defined in a single model. "Monitoring information obtained from the second polishing station during a current polishing cycle is used as feedback to adjust either the first or second polishing process of a subsequent polishing cycle." (Col. 4, lines 1-4). See also, Figure 5.Thus, only the metal polishing process is modeled and updated in the Bennett process.

Bennet does disclose polishing of an underlying dielectric layer at a subsequent station (see Fig. 6); however, in this example, the metal layer is removed at the first station (Step 604: "polish at [first station] at lower rate until underlying layer is exposed") and feedback information is generated at this point (Step 606: "generate feedback information for next polishing cycle"). The subsequent polishing of the dielectric step is not controlled by the model, as no feedback information is generated after polishing at the second polishing station.

Thus, Bennett discloses feedback control in a CMP process of a *single* layer of a wafer, e.g., the metal layer, and defines a processing recipe for that *single* layer of the wafer. There is no teaching or suggestion of a "model for CMP processing of a wafer having at least first and second layers" and a CMP model that provides "a first process recipe for the first process layer and a second process recipe for the second process layer," as recited in claim 1.

Similarly, Lee also lacks these features.

Lee provides "a method of controlling a polishing time of a next lot of wafers by using an algorithm for determining the variable removal rate from the relationship of chemical mechanical polishing (CMP) process data for *an actual patterned wafer of a previous lot* and the removal rate of a layer being polished on *a blanket wafer* essential for prediction of a CMP time." (Col. 2, lines 31-38.) The only reference to more than one layer in Lee is found when discussing the relationship "$\Delta ToxB = a^* \Delta ToxP + A$," which Lee defines as the relationship between a thickness variation ($\Delta ToxP$) for ***a layer on a wafer of the plurality of lots*** and a thickness variation ($\Delta ToxB$) for ***a layer on the blanket wafer***. (Col. 5, lines 24-29) According to Lee, "if the ***layers*** to be polished on the ***wafers*** of the plurality of lots are all formed of the same material, 'a' is substantially 1, while if two different layers to be polished are used, 'a' is expressed by the ratio of the removal rate between the two layers." (Col. 5, lines 29-34). Clearly, the layers referred to here are a single layer on each of the individual wafers being polished. There is no disclosure or suggestion of a ***single*** *wafer with multiple layers* or of a method of determining a polishing recipe for a multilayer wafer. Nor is there any suggestion to distinguish between multiple layers of a wafer in either a model or a measuring step.

In summary, the cited references, either alone or in combination, do not disclose or suggest numerous claim elements, including "a model for CMP processing of a wafer having at least first and second layers comprising at least one control parameter, said model comprising a first component that predicts a value for a characteristic of the first layer and a second component that predicts a value for a characteristic of the second layer"; and "polishing at least first and second layers of a wafer" using a process recipe based on the model. (claim 1)

Similar arguments apply to independent claims 10, 23 and 30.

Claims 2, 4, 6, 12, 13, 15, 17, 19, 24-26 and 29 depends directly or indirectly from claims 1, 10, 23 and 30, and are deemed to be allowable for the reasons discussed above as well as the additional limitations cited therein.

In view of the above, Applicants respectfully submit that claims 1, 2, 4, 6, 10, 12, 13, 15, 17, 19, 23-26, 29, and 30 are unobvious over the cited references and respectfully request that the rejection under 35 U.S.C. §103(a) of these claims be withdrawn.

C. Second Rejection under 35 U.S.C. §103(a)

Claims 3, 5, 7-9, 11, 14, 16, 18, 20-22, 27 and 28 are rejected under 35 U.S.C. §103(a) as being obvious over Bennett in view of Lee and further in view of Campbell et al. (US 6,230,069), hereafter "Campbell." The Office Action admits that nothing in Bennett and Lee teaches or suggests a specific model for the wafer characteristics, and argues that Campbell remedies these deficiencies. (Office action, page 5) Applicants respectfully traverse the rejection.

As an initial matter, claim 3 depends from claim 1 and is allowable for the reasons discussed above. Furthermore, there is no disclosure or suggestion of a wafer with multiple layers or of a method of determining a polishing recipe for a multilayer wafer. Nor is there any suggestion to distinguish between multiple layers of a wafer in either a model or a measuring step.

The Examiner refers to equation 13 in Campbell to assert that equation 13 is a short hand version of "$Y_t = Y_A + Y_B$, where $Y_t$ is the model for a CMP process for a multi-layer wafer; $Y_A$ is the model for a CMP process for the first layer of the wafer; and $Y_B$ is the model for a CMP process for the second layer of the wafer," as recited in claim 3. In contrast, equation 13 in Campbell is an optimization equation that defines "the difference between post-polish thickness at run k+j+1 and target post-polish thickness $y_T$" for a single layer (Col. 6, lines 51-52). Thus, the prior art does not show or suggest the combination of limitations recited in claim 3.

Campbell also does not disclose a model that "defines a plurality of regions on a wafer," as recited in claim 5. The examiner suggests that values a and b of equation 7 take into account the topology of the wafer. Campbell merely suggests that the coefficients "*a* and *b* can vary depending on the type of polishing tool, the table speed, the arm downforces, the slurry and the topography of the wafer being polished," and that the coefficients *a* and *b* are determined experimentally. However, Campbell neither teaches a model that "defines a plurality of regions

on a wafer" nor "a measured value for the wafer characteristic for each of the plurality of regions," as further claimed. Similar arguments apply for claims 16, 18 and 27.

Claims 3, 5, 7-9, 11, 14, 16, 18, 20-22, 27 and 28 depends directly or indirectly from claim 1, and are deemed to be allowable for reasons discussed above as well as additional limitations recited in each dependent claim also interpreted in combination.

In view of the above, Applicants respectfully submit that claims 3, 5, 7-9, 11, 14, 16, 18, 20-22, 27 and 28 are unobvious over the cited references and respectfully request that the rejection under 35 USC §103(a) of these claims be withdrawn.

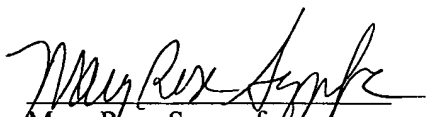
## AUTHORIZATION

The Commissioner is hereby authorized to charge any additional fees, which may be required for this Amendment, or credit any overpayment to deposit account no. 08-0219.

In the event that an extension of time is required, or which may be required in addition to that requested in a petition for an extension of time, the Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit any overpayment for an extension of time to deposit account no. 08-0219.

Respectfully submitted,

Dated: December 14, 2006



Mary Rose Scozzafava
Registration No.: 36,268
Attorney for Applicant(s)

Wilmer Cutler Pickering Hale and Dorr LLP
60 State Street
Boston, MA 02109
617-526-6000 (telephone)
617-526-5000 (facsimile)